Semiconductor Research Corporation

New Roadmap For Micro- And Nanoelectronics: Where the Semiconductor industry is headed over the next 5, 10, 20 years?

Victor Zhirnov
Chief Scientist
Victor.Zhirnov@src.org

Victor Zhirnov
Semiconductor Research Corporation

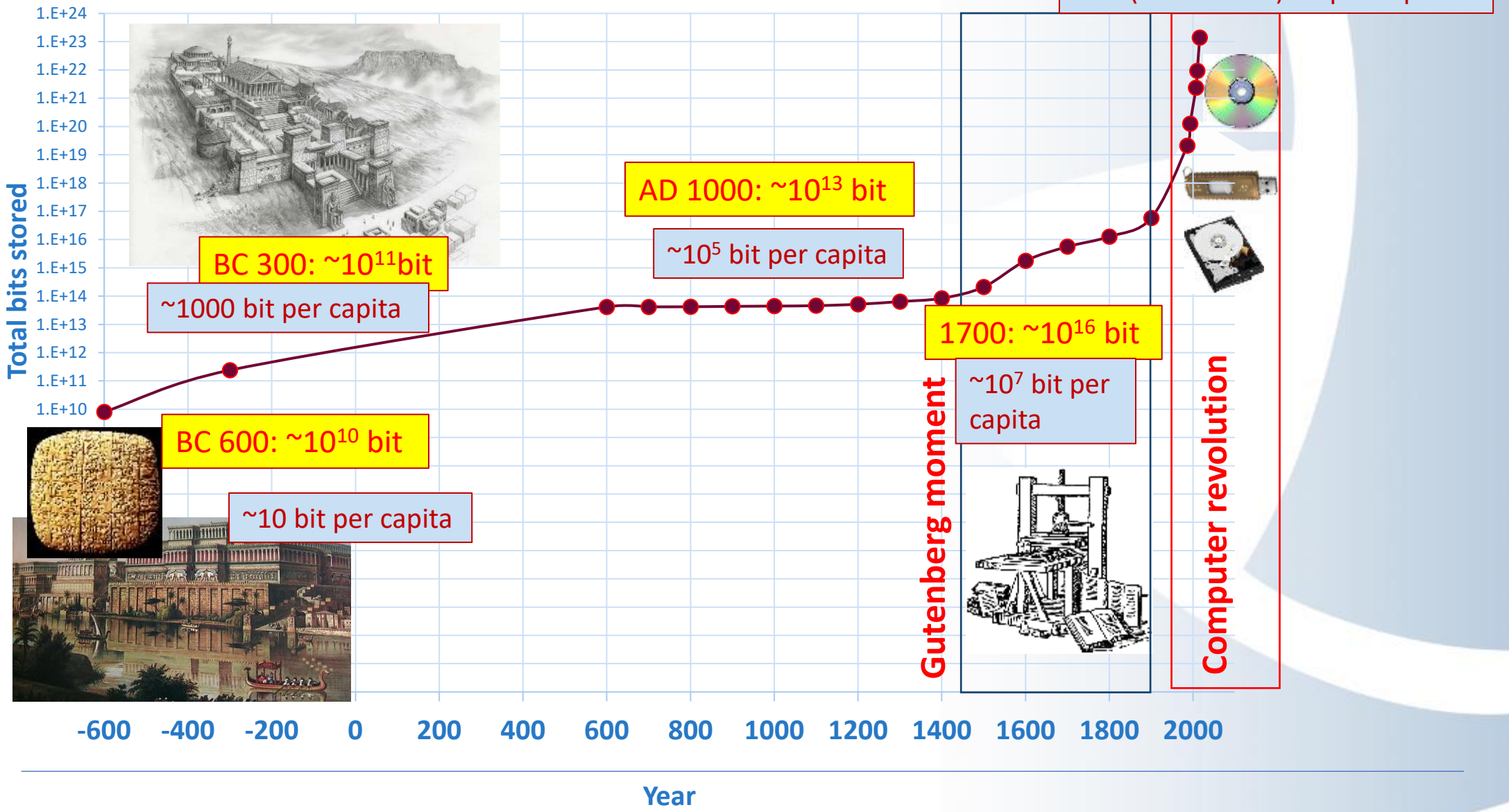
The 18th U.S.-Korea Forum on Nanotechnology:
Sensors Related to Human Cognition and Sustainability in Semiconductor Manufacturing

Outline

- Information is the Social-Economic Growth Engine of civilization
- Strategic Planning in Semiconductor Industry
  - International Technology Roadmap for Semiconductors (ITRS)
  - Decadal Plan for Semiconductors
  - Microelectronics and Advanced Packaging Technology Roadmap (MAPT)
- Semiconductor Needs after 2030 and the next microelelectronic revolution

Information is key for Human Augmentation!

Information along with Energy has been the Social-Economic Growth Engine of civilization since its very beginning



SRC

2020–2022 global chip shortage

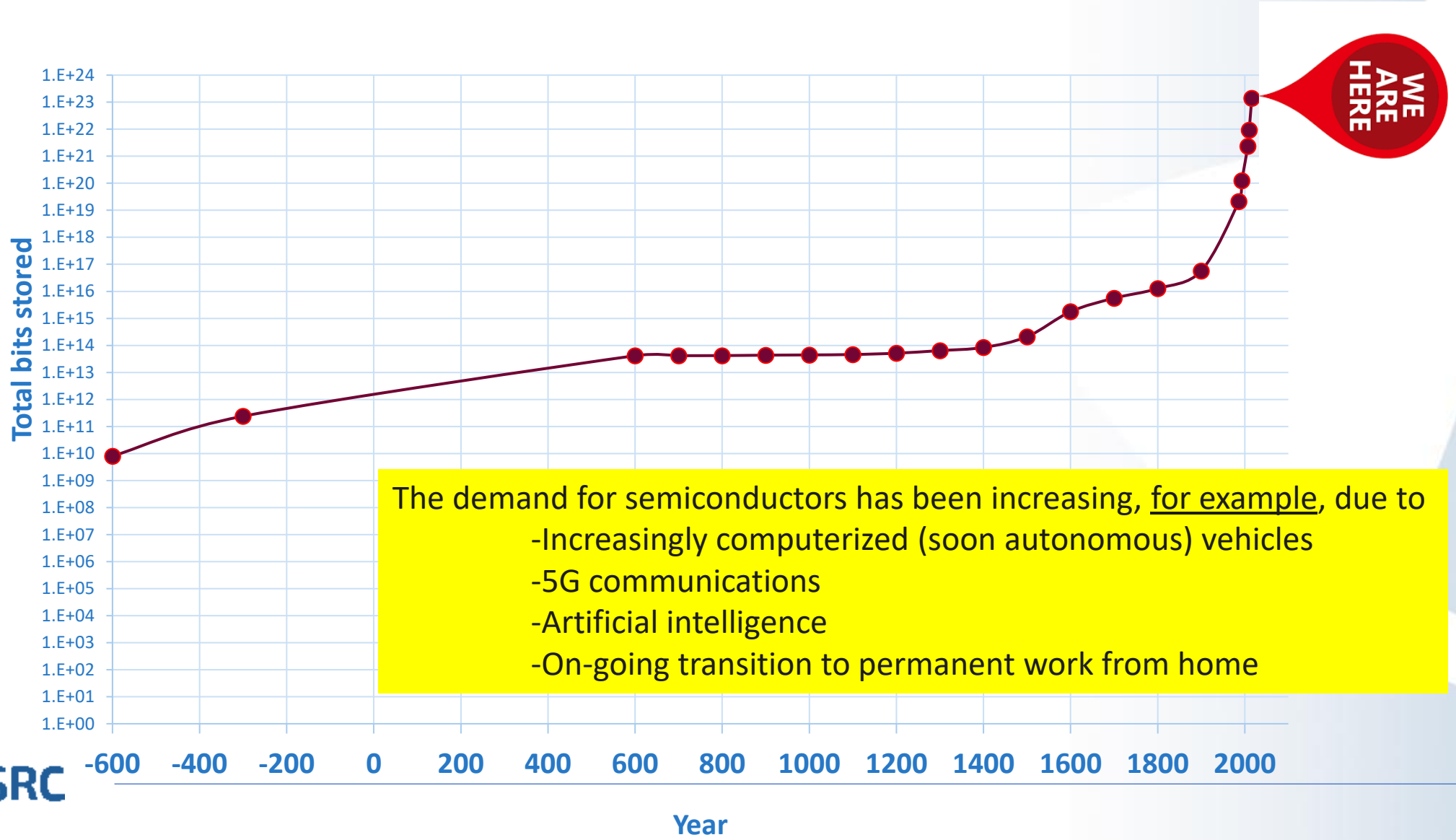
> *This is not a bubble. This is the oil crisis of 1973, but with chips*
>
> **Peter Wennink** – Topman ASML

What Caused the Global Chip Shortage?
'Simple' Reasons

- Pandemic
  - Government-mandated lock-downs forced several fabs to shut down temporarily
  - Automakers decided to cancel chip orders during 1Q20 and 2Q20 because of pessimistic demand prospects due to COVID-19

- Extreme Weather in Texas
  - In February 2021, Samsung, NXP and Infineon had to temporarily suspend plant operations for several weeks due to power failures in Austin, Texas, caused by major snowstorms, resulting in lost production

Main OBJECTIVE reason: accelerating demand for ICT resources



The demand for semiconductors has been increasing, <u>for example</u>, due to

- -Increasingly computerized (soon autonomous) vehicles
- -5G communications
- -Artificial intelligence
- -On-going transition to permanent work from home

SRC

Poor strategic planning was one cause of global chip shortage

- Semiconductor manufacturing has one of the highest R&D expenditures.
- Long manufacturing times. One chip has 1500 steps with hundreds of variables (about 20 weeks from start to finish)
- Workforce!!!
- Transnationality
  - materials/supplies are spread across many countriesStrong vendor lock-in
  - No of-the-shelf equipment on-demand

Strategic Planning in Semiconductor Industry

International Technology Roadmap for Semiconductors (ITRS)

- The MASTER PLAN of Semiconductor Industry.
  - A very detailed industrial perspective on the future requirements for microectronic technologies
    - Origin: SRC 10-y research goals
- Was built on worldwide consensus of leading industrial, government, and academic technologists
- Provided guidance for the semiconductor industry
  - Manufacturing
  - Design
  - Materials and equipment suppliers
- Engaged academic research worldwide
- **Was active for more than 20 y**

SRC

The Copper Revolution

Research Start: 1989

~10 years

Cornell, Berkeley, RPI, SUNY Albany

Commercialization: 1998-2002

Need:

Interconnects to:

1) break the **1GHz** barrier

2) reduce power

Challenge: Replace Al with Cu

- New deposition process
- Reliability (e.g. Cu diffusion and electromigration)

1st shipment - Sept 1998

AMD

SRC-funded basic research led to introduction of Cu interconnects in commercial products

SRC Cu Design Challenge
NOVELLUS • UMC GROUP
SpeedFam-IPEC

Turn copper into gold.

'Vendors'

APPLIED MATERIALS

NOVELLUS

TEL

Lam RESEARCH

SRC

Estimate of IBM's ROI from SRC's Interconnect program

- Program start – 1989
- 1st Commercialization – 1998 (IBM's PowerPC750 chip)
- Total SRC's investment in interconnects: **~$20M** (1989-1998)
- Total contribution per member :**~$1.3M** (1989-1998)
- IBM's revenues from PowerPC750 **through Sept.2000: ~$600M**
- **IBMs "ROI" ~ 460:1**

Thought Leadership That Positions Our Industry

2D Wafer Scaling

1st research roadmap across industry

1984 SRC 10y goals

1990 Microtech 2000

1992 SIA/SRC NTRS

1998 ITRS

National Technology Roadmap for Semiconductors

2015 STOP orphan years

Chip Crisis

2021 Decadal Plan for Semiconductors — 2030 Decadal Plan

Calls for3x increase of federal investments in semiconductors

2022 CHIPS for AMERICA

2023 MAPT

SRC's Decadal Plan

1987 SEMATECH

1999 SRC-MARCO

Massive DARPA-MTO investments in semiconductors

2005 SRC-NRI

Massive NSF and NIST investments in semiconductors

2017 SRC-JUMP SRC-nCORE

DARPA-ERI NIST

2023 SRC-JUMP 2.0

DARPA-ERI 2.0

3D Heterogeneous Integration

SRC

https://www.src.org/about/decadal-plan/

Five "Seismic Shift" Research Priorities

- Smart Sensing — **The Analog Data Deluge**
- Memory & Storage — **The Growth of Memory and Storage Demands**
- Communication — **Communication Capacity vs. Data Generation**
- Security — **ICT Security Challenges**
- Energy Efficiency — **Compute Energy vs. Global Energy Production**

SRC

By design, the Decadal Plan focuses on WHAT to accomplish, not HOW to accomplish it.

Microelectronics and Advanced Packaging Technologies (MAPT) Roadmap

https://srcmapt.org/

SRC

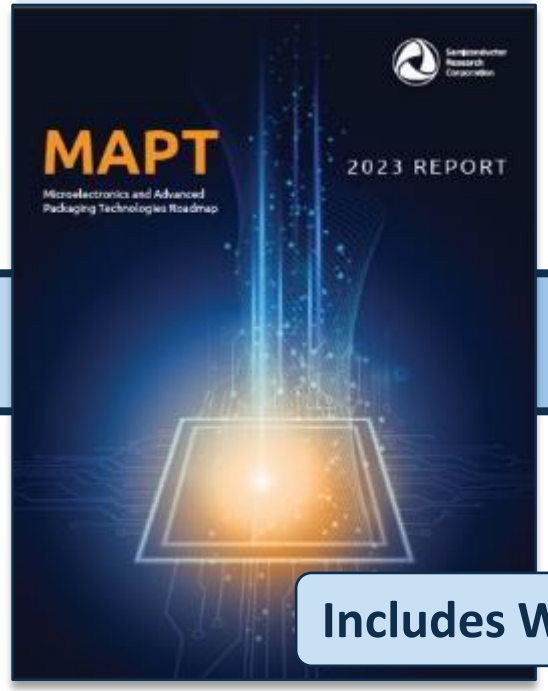
The Industrial Roadmap

The What

January 2021
2030 Decadal Plan for Semiconductors

181 participants
81 organizations

The How



Includes WFD

October 2023
Microelectronics & Advanced Packaging Technologies (MAPT) Roadmap

300 participants
112 organizations

The Implementation

CHIPS for AMERICA

2024+
CHIPS and SCIENCE Act – 9903 and 9906 R&D Investments

www.nist.gov/chips

Press

Press

Needs and Drivers

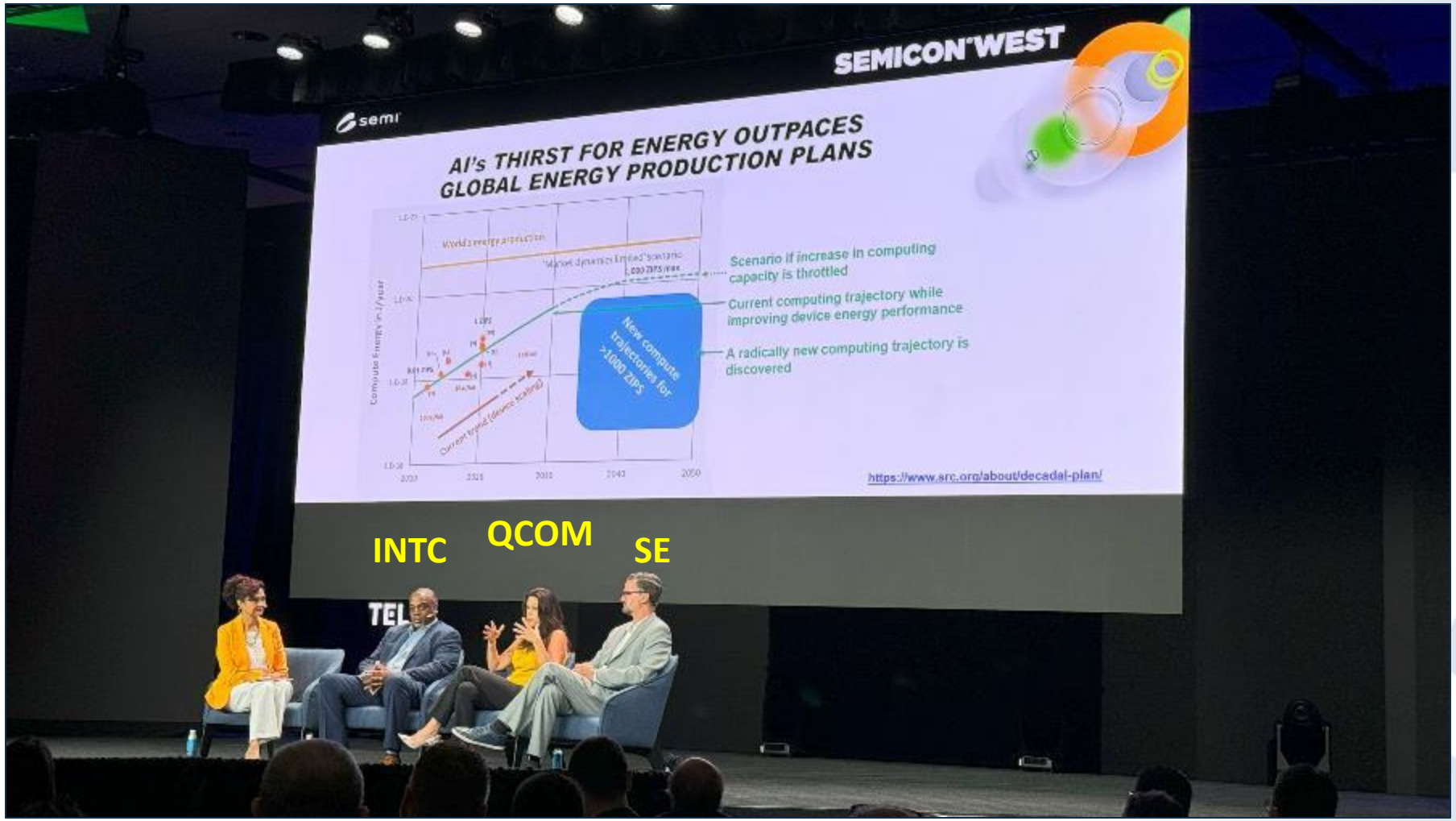
Needs: Decadal Plan for Semiconductor

Drivers: MAPT Roadmap

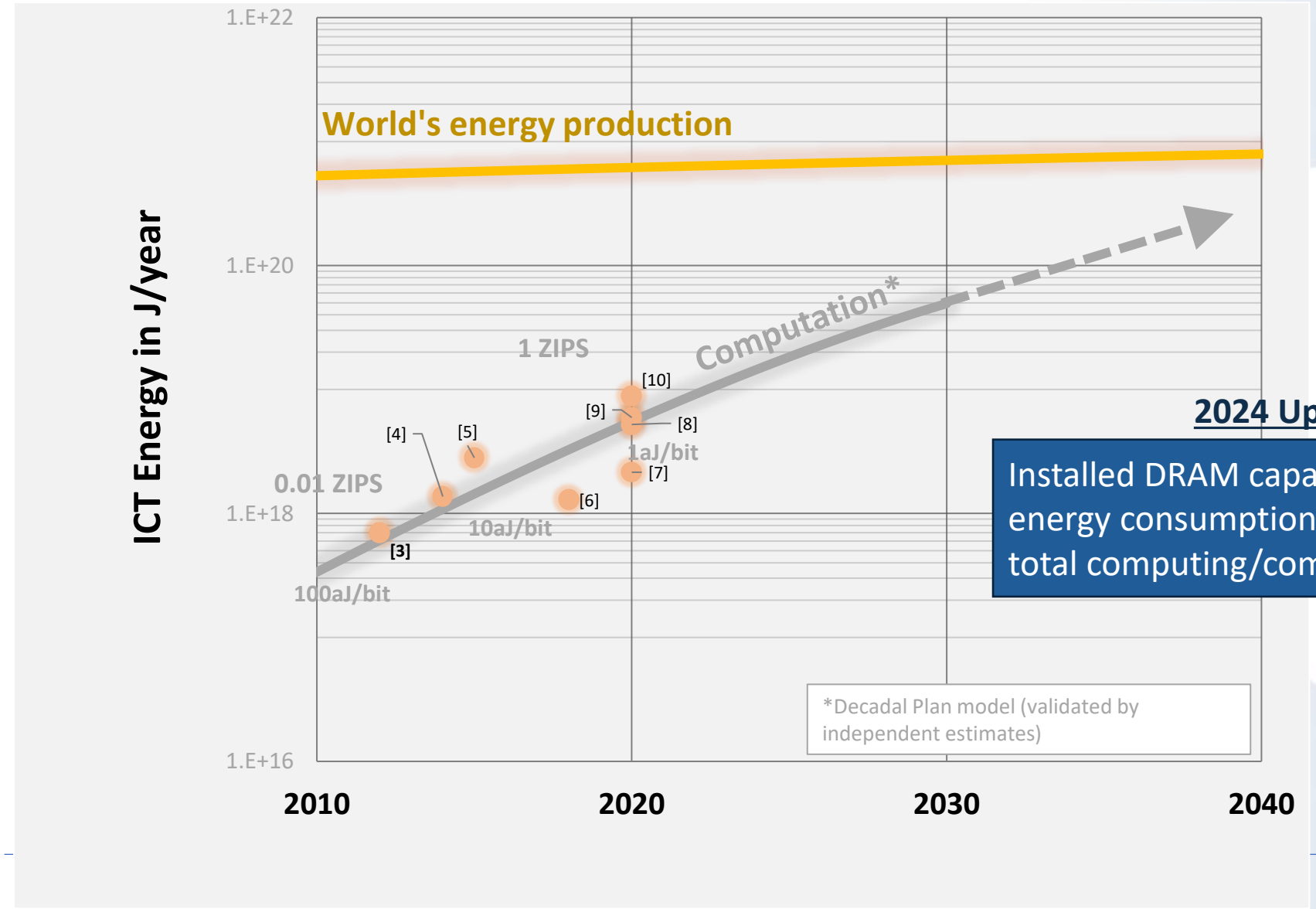
- Artificial Intelligence, HPC
- Automotive,
- Mobile, biomedical, & security

SRC

Sustainability and Energy Efficiency



ICT Energy (computation) in 2021



2024 Update

Installed DRAM capacity and its energy consumption as a proxy for total computing/computing energy

SRC

The Washington Post
Democracy Dies in Darkness

BUSINESS

Amid explosive demand, America is running out of power

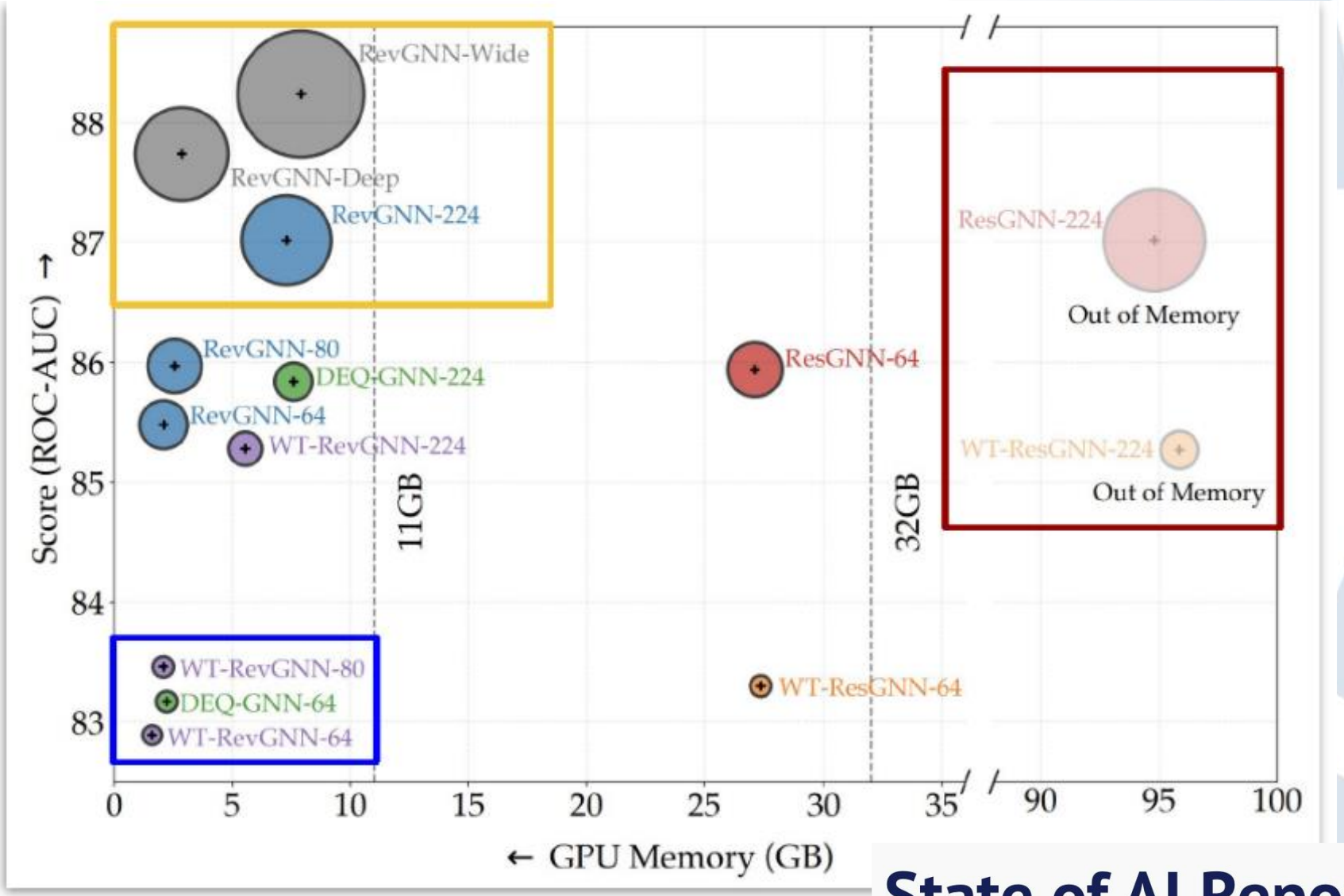
AI and the boom in clean-tech manufacturing are pushing America's power grid to the brink. Utilities can't keep up.

By Evan Halper

March 7, 2024 at 6:05 a.m. EST

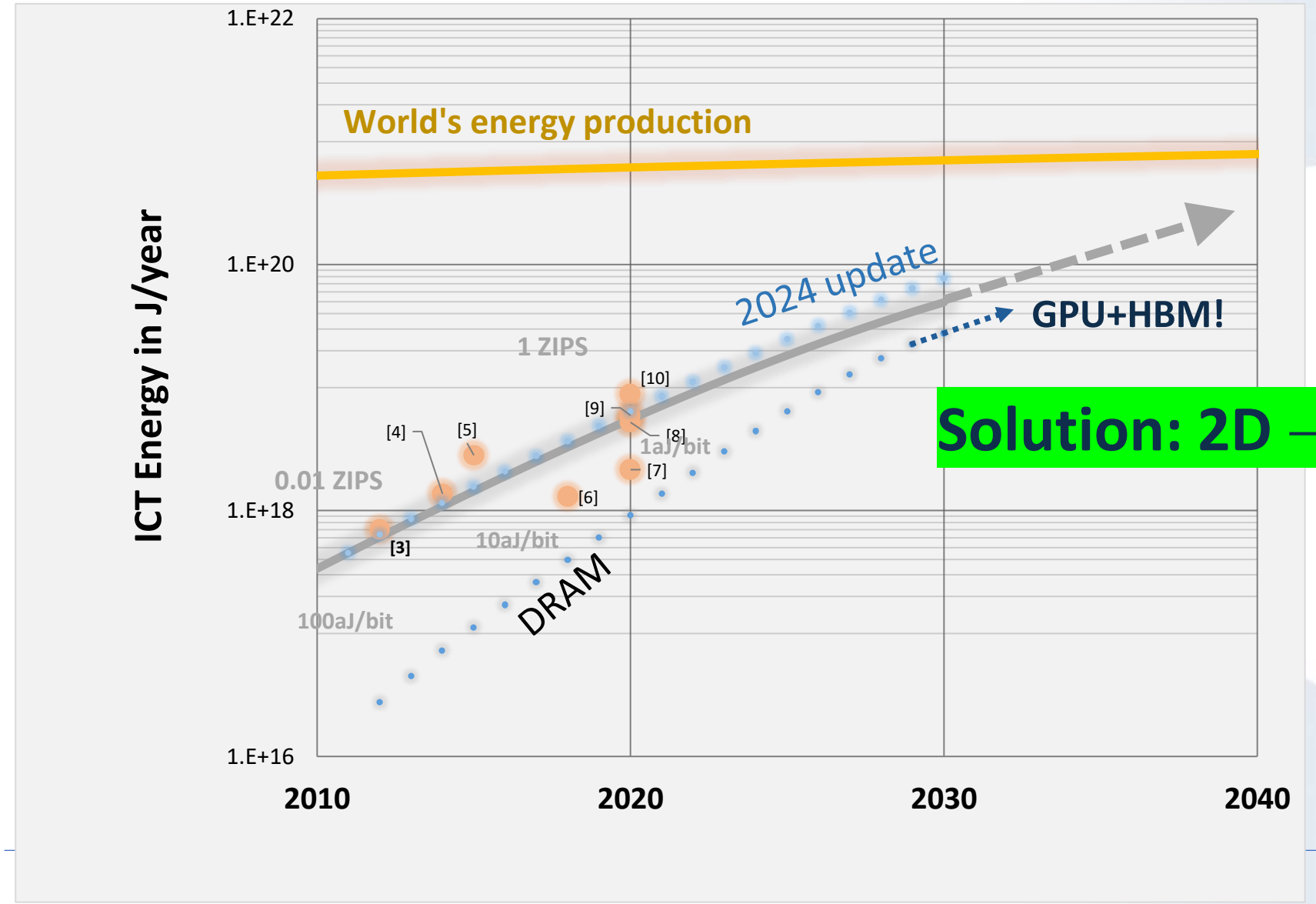
DRAM consumption in AI

Source: Matthias Müller
Intel Labs – Munich, Germany



State of AI Report 2021

ICT Energy (computation)



SRC

MAPT Highlights: Sustainability and Energy Efficiency

1 Need: 1000x → 100000x increase in computing energy efficiency over the next 2 decades (per Decadal Plan)

2a Opportunity: Advanced Packaging supports tighter integration of xPU+memory+photonic interconnects & I/Os

2b Opportunity: Analog Renaissance in Data Processing at the Edge

3 2022 data: 5.3B cell phones were thrown away. Overall, ~ 60M tons of e-waste was disposed and less than 20% was recycled

4 DfS=Design for Sustainability!

SRC

Chapter 2: Sustainability and Energy Efficiency

Continue developing new and beneficial technologies, while simultaneously ensuring environmental considerations are an integral part of the product lifecycle to help decrease the overall environmental impact of microelectronics.

Manufacturing:
- Energy and water consumption
- GHG emissions
- Chemicals and material use
- Refinement of materials
- "Greener" chemistries and processes

Emissions/ Releases:
- Benign in the environment
- Non-toxic
- No / Low GWP, ODP, etc.
- Transformed, or transformable to benign end products

Recycle

Reuse

Raw materials, chemicals, energy

Synthesis of materials & processes for SC supply chain

Device Mfg

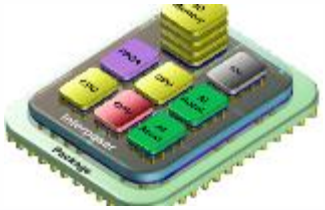
Recycle or Treatment of fab mfg wastes/effluents

Air

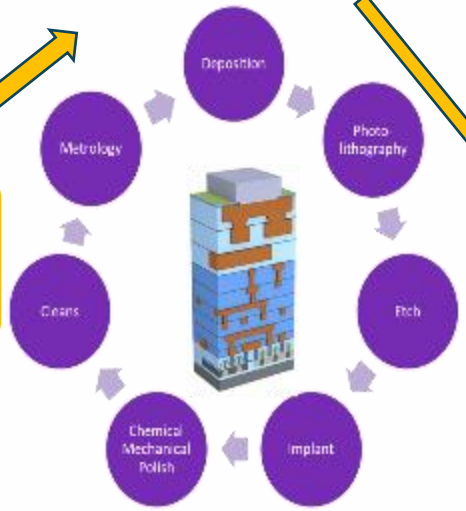
Water

Waste

Device and System Design:
- Efficient manufacturability with benign materials and processes
- Low energy use, high value
- Recyclability
- Chiplets designed for reuse and repair
- Energy efficient heterogeneous computing via Chiplet ecosystem



Device/ Product Design



Device/ Product Use

Reuse/ Refurbish/ Recycle

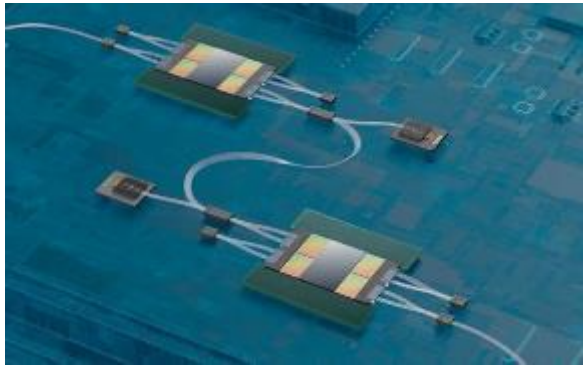
Product Use
- Energy Efficiency
- Water for cooling
- Energy distribution loss

End-of-life
- E-waste
- Chemicals
- Rare earth metals

Recycle

Need: 1000x Power Reduction (at least)!

- Achieving significant energy efficiency requires
  - 3D chips
    - Use of chiplets and HBM in AI/ML, graphics, HPC, and communication
    - Memory and processing integration to meet high-bandwidth and low-latency demands
  - Photonics I/O



- All of the above requires Advanced Packaging
  - Advanced Packaging is New King!

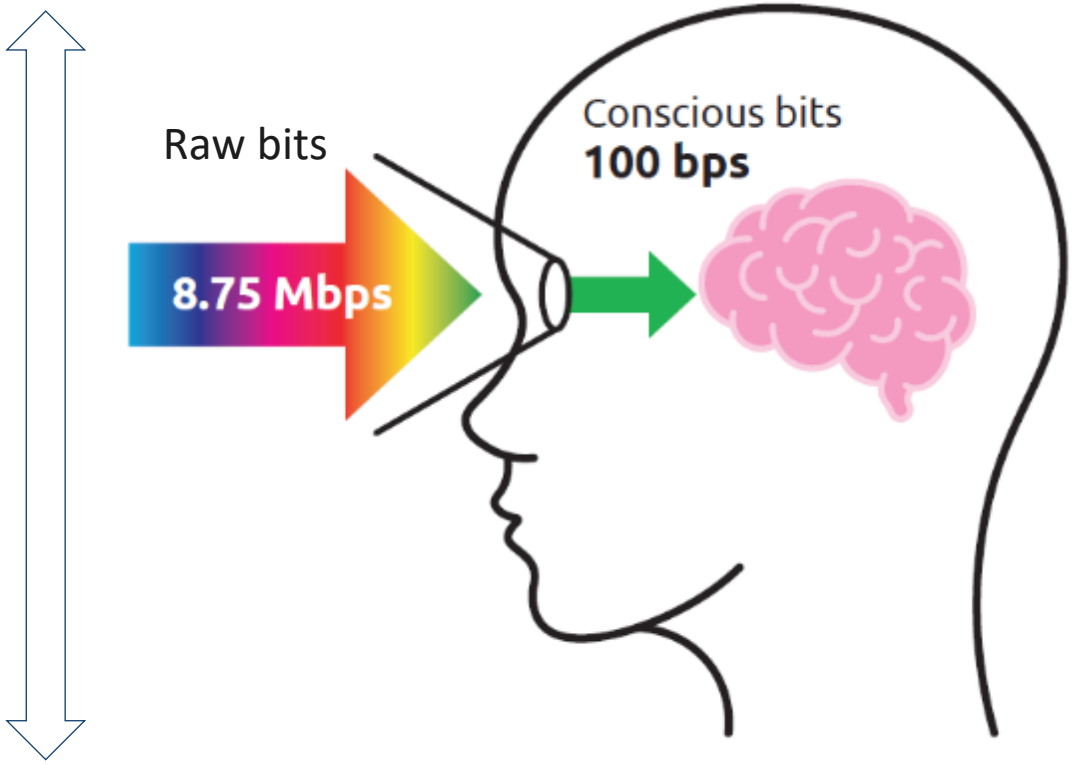
Advanced Packaging, along with 2.5D/3D heterogeneous integration, will be the key enabler of the next microelectronic revolution. In fact, advanced packaging+3D is becoming the equivalent of transistor of the Moore's Law and ITRS era.

SRC

Enablement Components to System I: Analog Renaissance in Data Processing at the Edge

- Analog signal processing for energy efficiency
- Pre-processing data at the edge for efficient data handling

Compression ratio: 100,000:1



An example of 'Analog Goal' for 2030:

- UltraCompressed Sensing (UCS), e.g.
- Analog-to-Information converters with practical compression ratio of 10^5:1

Typical MPEG-4 lossy compression video: 100:1

Needs and Drivers

Needs: Decadal Plan for Semiconductor

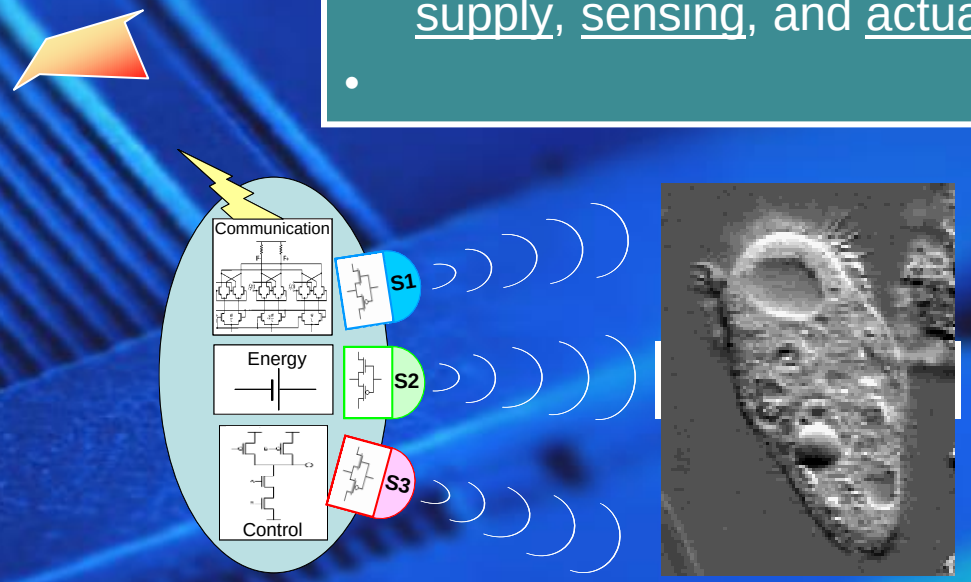
Drivers: MAPT Roadmap

- Artificial Intelligence, HPC
- Automotive,
- Mobile, biomedical, & security

SRC

Gedanken '*In Silico*' System

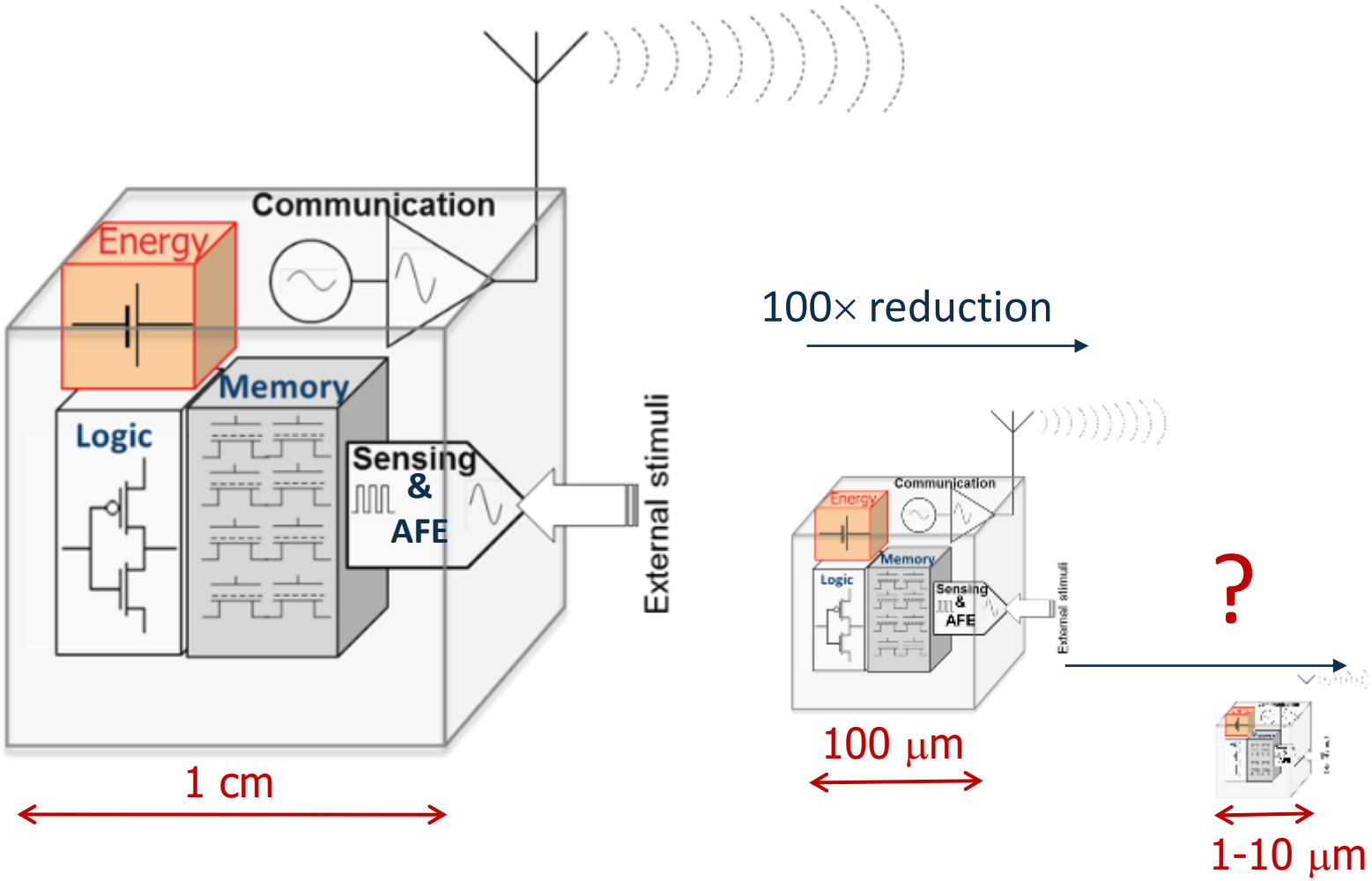
- **Nanomorphic Cell:** A model system, designed to analyze the physical scaling limits of electronic systems,
- Postulated to be confined within a 10μm×10μm×10μm cube.
- An atomic-level integrated, self-sustaining microsystem with **six** primary components: computation, communication, energy supply, sensing, and actuation.
-



Benchmark: Living cell
***In carbo* system**

"Microsystems for Bioelectronics: The Nanomorphic Cell", by Victor V. Zhirnov and Ralph K. Cavin (*Elsevier*, 2010)

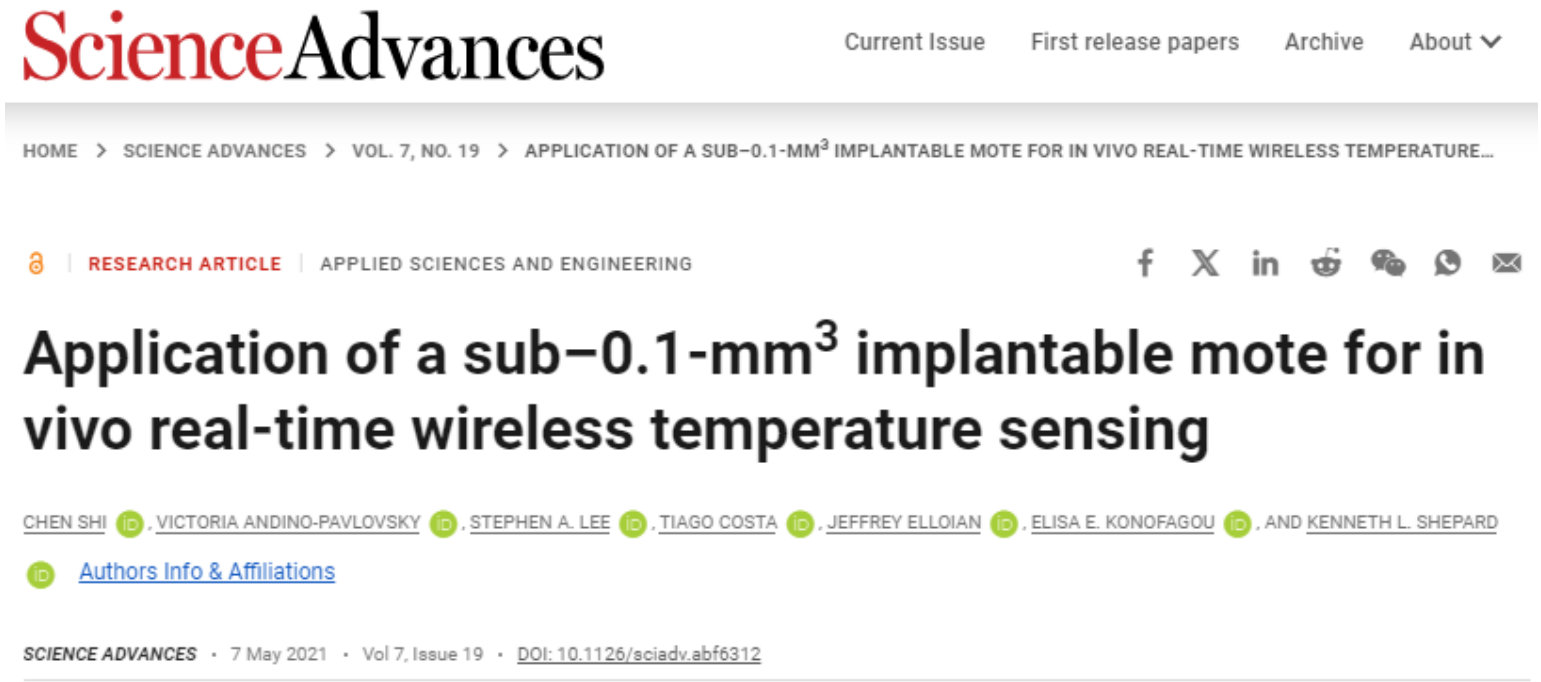
Miniaturization:
Design Trade-offs and Fundamental Physical Limits



Elsevier 2015

Directly link nanoelectronics sensors and processors to biological systems in such a way as to comprehend and leverage bio-information processing systems to provide new bio/nano-electronic medical protocols to enhance human health.

SRC



Science Advances

Current Issue First release papers Archive About

HOME > SCIENCE ADVANCES > VOL. 7, NO. 19 > APPLICATION OF A SUB–0.1-MM^3 IMPLANTABLE MOTE FOR IN VIVO REAL-TIME WIRELESS TEMPERATURE...

RESEARCH ARTICLE | APPLIED SCIENCES AND ENGINEERING

Application of a sub–0.1-mm^3 implantable mote for in vivo real-time wireless temperature sensing

CHEN SHI, VICTORIA ANDINO-PAVLOVSKY, STEPHEN A. LEE, TIAGO COSTA, JEFFREY ELLOIAN, ELISA E. KONOFAGOU, AND KENNETH L. SHEPARD

Authors Info & Affiliations

SCIENCE ADVANCES · 7 May 2021 · Vol 7, Issue 19 · DOI: 10.1126/sciadv.abf6312

MAPT Roadmap

- Biological use cases have stringent packaging requirements
  - Miniaturization, especially for systems that require small form factor to unlock new use cases, like biological sensors
  - Integration and packaging for continuous exposure of liquids or biological samples to sensor in integrated package

SRC

The Stage is Set for an Industrial Renaissance…SRC's Call to Action!

- The current hardware paradigm must shift to create the desired value with heterogeneity from **3D microelectronic and advanced packaging technologies (MAPT)** as the key driver.
- To stay at the leading edge of hardware innovation, we must invest in early-stage ideas and tech maturation, exploring key options through a **fast-fail and tech-transfer mindset**.
- We must be committed to workforce development and broadening participation. There is a bright future for semiconductors, but **we must change our narrative** to win over the hearts and minds of next gen innovators.

The greatest risk is not investing in semiconductor technology and people for our collective future

Acknowledgement: All contributors to the MAPT Roadmap

300 participants
112 organizations

SRC